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Design and Verification of Advanced Carry Select Adder

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Abstract
Design ofareaefficient data pathlogicsystems formsthelargestareasofresearch inVLSIsystem design.Indigital adders, thespeed of addition islimitedbythetimerequired totransmit a carrythroughtheadder.CarrySelectAdder (CSA) isoneofthefastestadders usedinmanydata-processingprocessorstoperform fastarithmetic functions. Fromthestructure oftheCSA,itisclear thatthereisscopeforreducing thearea and powerintheCSA. This work usesasimpleandefficient gate-level modification todrasticallyreducetheareaandpower oftheCSA.Basedonthismodification 16,32,64 and128-bitsquare-root CSA(SQRT CSA) architectureshavebeendevelopedandcomparedwith theregularSQRTCSAarchitecture. Theproposed designhasreducedarea and powerascompared withtheregular SQRTCSA.Thisworkestimates theperformanceof theproposed designsintermsofpower,areaand isimplementedusingXilinxISE and synthesized using cadence in 90nm technology.

Keywords-CarrySelectAdder,Area, Power, SQRT.

I. INTRODUCTION

Inrapidly growingmobileindustry,fasterunitsarenottheonly concern butalso smaller areaand lesspowerbecome majorconcernsfordesignofdigitalcircuits.Inmobileelectronics, reducing areaandpowerconsumptionarekeyfactorsin increasingportability andbatterylife.Eveninserversand desktopcomputers powerdissipationisanimportantdesign constraint.Designof areaandpower-efficienthigh-speeddata pathlogicsystemsare one of themostsubstantialareasof researchinVLSIsystem design.Indigitaladders,thespeedof additionislimitedby thetimerequiredtopropagateacarry through the adder. The sumfor each bit positionin an elementary adder is generated sequentially only after the previous bitpositionhas beensummedanda carry propagated intothe nextposition.Amongvariousadders,theCSA is intermediate regardingspeedandarea.

Additionistheheartof computerarithmetic,and thearithmetic unitisoftentheworkhorseofacomputationalcircuit.They are thenecessarycomponentofadatapath,e.g.inmicroprocessors orasignalprocessor.Therearemany waystodesignanadder. The Ripple Carry Adder(RCA) providesthe mostcompact designbut takeslongercomputingtime. If thereisN-bitRCA, thedelayislinearlyproportionaltoN.Thusforlargevalues of NtheRCAgiveshighestdelayofalladders.TheCarryLook-AheadAdder(CLA)givesfastresultsbutconsumeslargearea. IfthereisN-bitadder,CLAisfastforN ≤4,butforlargevalues ofN bitsdelay increasesmorethanotheradders.Soforhigher numberof bits,CLAgiveshigherdelaythanotheraddersdueto presence of large numberoffan-inandalarge numberof logic gates.TheCarry SelectAdder(CSA)providesacompromise betweensmallareabutlongerdelay RCAandalargeareawith shorter delayCLA.

In this paper the design of Modified CarrySelect-Adder (MCSA) and Uniform carry select adder (UCSA)architectures toreduce area andpowerwithminimum speedpenalty is described .TheMCSA and UCSA isdesignedby usingsingleRCAand Binary to Excess-1 Converter(BEC) and Carry skip adder (CSKA).

II. BASICADDERBLOCK

TheadderblockusingaRipplecarry adder, BECandMuxisexplainedinthissection. In this we calculate andexplainthedelay &areausingthe theoretical approachand showhowthedelayand areaaffectthe totalimplementation.The AND,OR, andInverter(AOI)implementationofanXORgate isshowninFig.1.Thedelay andareaevaluation methodology considersallgatesto bemadeupof AND,OR,andInverter,eachhavingdelayequalto1 unitandareaequalto 1unit.Wethenaddupthe numberofgatesinthelongestpathof alogicblock thatcontributesto themaximumdelay.Thearea evaluationisdone bycountingthe totalnumberof AOIgatesrequiredforeachlogicblock.Basedon thisapproach, theblocksof2:1mux,HalfAdder (HA),andFAareevaluatedandlistedinTableI.

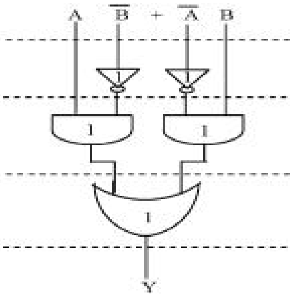


Fig. 1:DelayandArea evaluationofanXORgate.

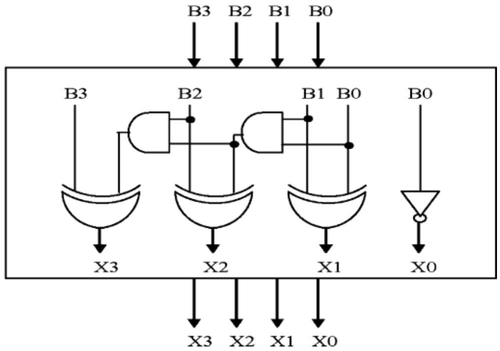


Fig.2:4-bBEC.

The Booleanexpressionsof the4-bit BECis listedas(notethefunctionalsymbols~NOT,&AND, ^XOR)

X0= ~B0
X1= B0^B1
X2= B2^(B0&B1)
X3= B3^(B0&B1&B2)

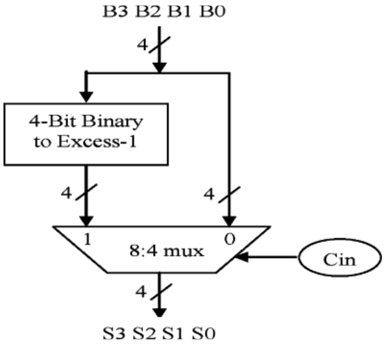
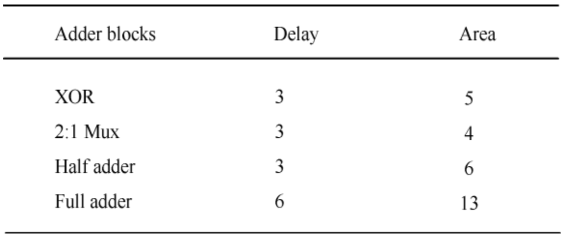


Fig.3:4-bBECwith8:4mux.



Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

Table 1: Delay and Area count of Basic Blocks of CSA

Thebasic workistouseBinaryto Excess-1Converter (BEC)insteadofRCAwithC_{in}=1in theregularCSA toachievelowerareaandpower consumption. ThemainadvantageofthisBEClogic comes fromthelessernumber oflogic gatesthanthen-bit FullAdder(FA)structure.Asstatedabovethemainidea ofthisworkistouse BECinsteadoftheRCAwithC_{in}=1 inordertoreducetheareaandpowerconsumptionofthe regularCSA. Toreplacethen-bitRCA,ann+1-bitBEC isrequired. Astructure and the function tableofa4-bit BECareshowninFig.2.

III. BASICSTRUCTUREOF REGULAR16-BIT CSA

A16-bitcarryselectaddercanbedeveloped intwodifferentsizesnamely uniformblocksizeand variableblocksize.Similarlya32,64and128-bit can alsobe developedintwomodesof different blocksizes.Ripple-carry addersarethesimplestand mostcompactfulladders,buttheirperformance is limitedbyacarrythatmustpropagatefromtheleast-significantbittothe most-significantbit.Thevarious 16,32,64and128-bitCSAcanalsobedeveloped byusingripplecarryadders.Thespeedofacarry-selectaddercanbeimprovedupto 40%to 90%,by performingthe additionsinparallel,andreducingthe maximum carrydelay.

Fig. 4showstheRegularstructureof 16-bit SQRTCSA.Itincludesmanyripplecarryaddersof variablesizeswhicharedividedinto groups.Group0 contains2-bitRCAwhichcontainsonly oneripple carry adderwhichaddstheinputbitsandtheinput carry andresultstosum[1:0]andthecarry out.The carry outoftheGroup0whichactsastheselection inputto muxwhichisingroup1, selectstheresult fromthe correspondingRCA(C_{in}=0)orRCA (C_{in}=1).Similarly the remaininggroupswillbe selected dependingontheC_{out} fromtheprevious groups.

InRegularCSLA,thereisonly oneRCAto performtheadditionoftheleastsignificantbits[1:0]. The remainingbits(otherthanLSBs),the additionis performedby usingtwoRCAscorrespondingtothe one assumingacarry-inof0,theotheracarry-inof1 withinagroup.Inagroup,thereare twoRCAs that receivethesamedata inputsbutdifferentC_{in}. The actualC_{in}fromthepreceding sector selects one of the two RCAs. That is, as shown in Fig. 4, if the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of lower RCA is selected.

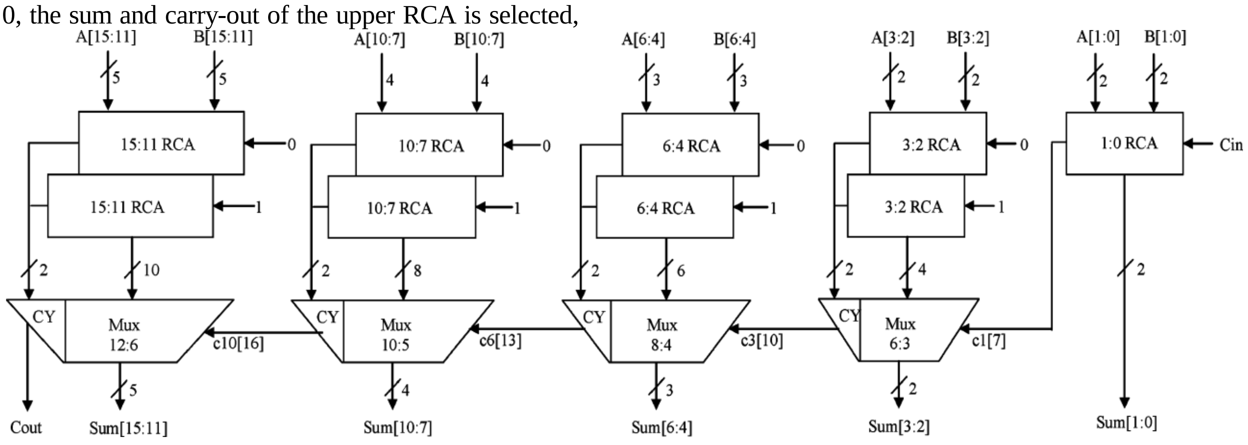


Fig.4:Regular16-bSQRTCSA.

IV. BASIC STRUCTURE OFMODIFIED 16-BIT CSA

This architectureissimilartoregular64-bit SQRTCSA,theonly changeisthat,wereplace RCAwithC_{in}=1amongthetwoavailableRCAsin agroupwithaBEC. ThisBEChas afeaturethatit canperformthe similaroperationasthatofthe replaced RCA with Cin=1. Fig 6shows theModified blockdiagramof 16-bit SQRTCSA. The numberofbitsrequiredforBEClogicis1bit more than theRCAbits. The modified block diagramis alsodividedintovariousgroupsof variablesizesofbitswith each grouphavingthe ripplecarry adders, BEC andcorrespondingmux.The basic BEC is shown in Fig. 3. As showninthe Fig.5,Group0containoneRCA onlywhichis havinginputof lowersignificantbit andcarry inbitandproducesresultofsum [1:0] andcarryoutwhichisactingasmuxselectionlinefor thenextgroup, similarlytheprocedurecontinuesfor highergroupsbuttheyincludesBEClogicinsteadofRCA withC_{in}=1.Basedontheconsiderationof delayvalues,thearrivaltimeofselectioninputC1 of8:3muxisearlierthanthesumofRCA andBEC. Forremaininggroupstheselectioninput arrivalis laterthantheRCA andBEC.

Thus, thesum1andc1 (output from mux) dependson mux and results computed byRCAand BEC respectively. The sum2 depends on c1 and mux. For theremainingpartsthearrivaltimeof muxselection inputisalwaysgreaterthanthearrivaltimeof data inputsfromtheBEC's.Thus,thedelay ofthe remainingMUXdependsonthearrivaltimeofmux selectioninputand themuxdelay.InthisModified CSA architecture, the implementation codeforFullAdderandMultiplexersof6:3,8:4,and10:5up to24:11weredesigned.Thedesign codefor theBECwasdesignedby usingNOT,XORandAND gates.Then2, 3,4,5upto11-bitripplecarryadder wasdesigned.

V. BASIC STRUCTURE OF UNIFORM16-BIT CSA

InthisUCSLA,carryskipadder(CSKA)is usedforreducing delayand areacomparedwithregular and modified CSA.Theupperadderhas theCSKA withC_{in}=0andtheBECcircuitisinthelower adderinsteadofRCAwithC_{in}=1intheUCSA.The 16 bit UCSA architecture isshowninFig.7.The CSKA shown in Fig.5isusedtoreducethedelay comparedwithRCA.Thegroup1has onlyone set of4bitCSKAwithcarry-in signal.The carry-outoftheCSKA isusedas controlsignalin multiplexer.Thegroup2hasonesetof4bitCSKAwithC_{in} =0 andonesetof5bitBECinsteadof4bitCSKAwithC_{in}=1.

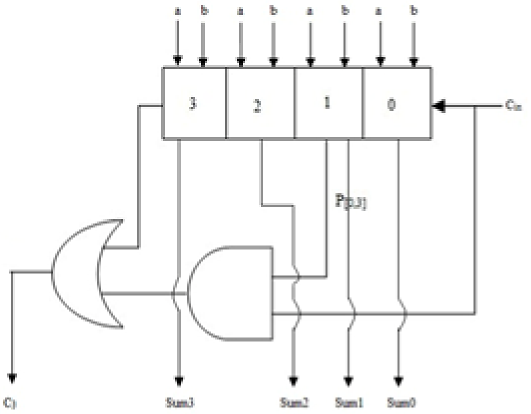


Fig 5: 4 bit CSKA Architecture

VI. IMPLEMENTATION RESULTS

Thedesignproposed inthispaperis developedusingVerilog-HDL inXilinx ISEandsynthesizedusing cadence in 90nm technology.Foreachwordsizeoftheadder, theVerilog code is dumped into cadence toperformthepowersimulations. The similardesign flowisfollowed forboththemodified and uniformSQRTCSA.Fig 8 exhibitsthesimulation resultsof16-bitCSA structures and Table 2 distinguish themin termsof Delay and Area.

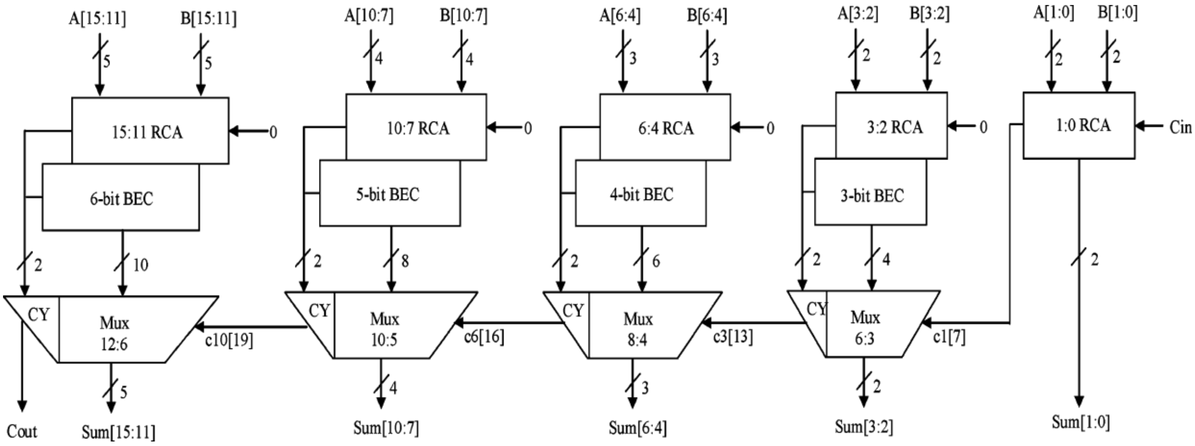


Fig.6: Modified16-bSQRT CSA – TheparallelRCAisreplacedwithBEC

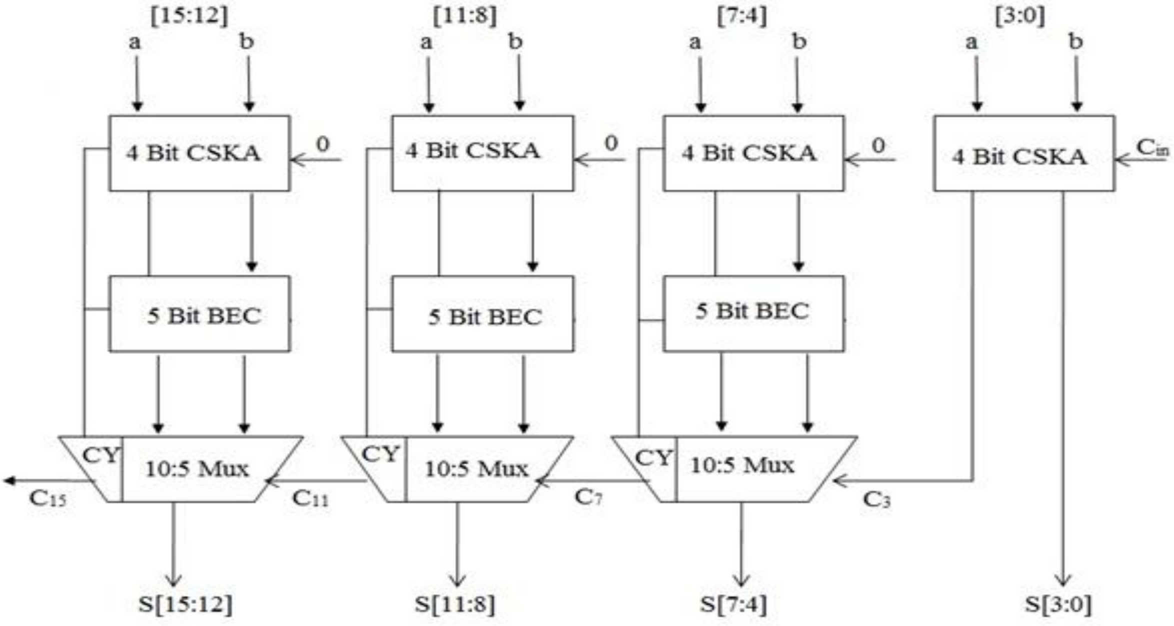


Fig.7: Uniform 16-bit SQRT CSA- The parallel RCA is replaced with BEC and CSKA

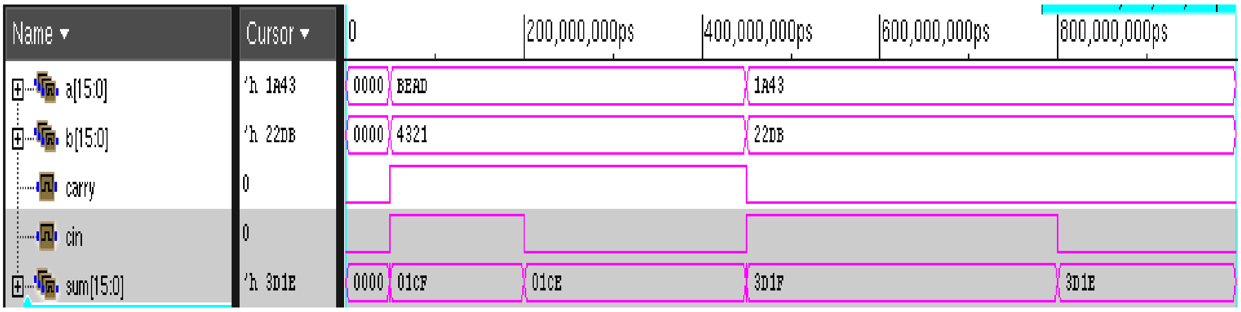


Fig. 8: 16-bit CSA output Waveform

S.No.	Adders		Power (nw)	Area (μm^2)
1.	16–bit	Regular	32803.4	652
		Modified	31585.5	562
		Uniform	29871.4	528
2.	32–bit	Regular	69970.6	1356
		Modified	63658.8	1156
		Uniform	63108.8	1128
3.	64–bit	Regular	143885.5	2805
		Modified	131386.0	2387
		Uniform	125165.7	2327
4.	128–bit	Regular	311320.8	5719
		Modified	276443.4	4844
		Uniform	257825.0	4724

Table 2: Comparisons of Regular, Modified and Uniform CSA

VII. CONCLUSION

The synthesis and simulation of Regular Square Root Carry Select Adder(SQRTCSLA),ModifiedSquareRootCarry SelectAdder and Uniform Square Root Carry Select Adder wasdonein VerilogHardwareDescriptionLanguageusingXilinxISEtool and Synthesis is done using Cadence.Acarry-selectadder is a particular way to implement anadder in which a logic element thatcomputesthe (n+1)bitsumoftwo n -bitnumbers and also replacing Ripple Carry Adder with Carry Skip Adder.

Theapproachproposedinthisreport is toreducetheareaandpowerofSQRT CSLAarchitecture.Thereducednumberofgatesofthisworkoffersgreatadvantage inthereductionofareaandtotalpower. But minimization of delay was not possible using the proposed architecture. The compared results show that the area and power of 128-bit Uniform SQRT CSLA are significantly reduced by 17.39% and 17.18% respectively. Similarly, the area and power of 128-bit Modified SQRT CSLA are significantly reduced by 15.29% and 11.20% respectively which indicates the success of the method for power and delay. The power-delay Product and Area-Delay Product of the proposed design varies for 16-, 32-, 64-, 128-bit sizes

The Uniform SQRT CSLA Architecture is therefore low power, low area, simple and efficient for VLSI hardware implementation. It would be interesting to design a SQRT CSLA Architecture which has reduced delay. In futurepower utilization, area and also delay can bereduced greatlybyusing various adders in Carry Select Adder Architecture.

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